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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,654	01/12/2001	Donnie W. Woods	100630.53029US	2274

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EXAMINER	
NGUYEN, SIMON	
ART UNIT	**PAPER NUMBER**
2685	7

DATE MAILED: 02/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/759,654	WOODS ET AL.	
	Examiner	Art Unit	
	SIMON D NGUYEN	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 13-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-10, 13-20, 22-29, 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vorenkamp et al. (6,591,091) in view of Dacus et al. (6,172,579).

Regarding claim 1, Vorenkamp discloses a phase detector for generating a phase error signal indicative of a phase difference between a reference signal and an oscillator signal (figs. 17-18), comprising: an amplifier to convert said reference signal to a substantially square wave signal (column 23 lines 2-22); and a phase detector to generate said phase error signal from said substantially square-wave signal and said oscillator signal (figs. 17-18, column 25 line 51 to column 26 line 67). It should be noted that Vorenkamp discloses that output signals are sampled and feed-backed in order to stabilize the output signals (column 24 lines 5-9, 25) which means the phase detector is a sampling phase detector. However, Vorenkamp does not specifically disclose a sampling phase detector.

Dacus, in the same kind of invention, discloses a PLL frequency synthesizer (abstract, fig. 19) wherein the PLL including a sampling phase detector (column 21 line

45 to column 22 line12). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have Vorenkamp, modified by Dacus to check errors may happen in each pulse in order to prevent the loop from responding to the modulation induced phase error.

Regarding claim 4, Vorenkamp discloses a phase detector for generating a phase error signal indicative of a phase difference between a reference signal and an oscillator signal (figs. 17-18), comprising: an amplifier to convert said reference signal to a substantially square wave signal (column 23 lines 2-22); a phase detector to generate said phase error signal from said substantially square-wave signal and said oscillator signal (figs. 17-18, column 25 line 51 to column 26 line 67); and buffers 1352,1354,1356 as transformers to transform an input signal to an balanced output (very low jitter getter output (column 22 line 52-56). It should be noted that Vorenkamp discloses that output signals are sampled and feed-backed in order to stabilize the output signals (column 24 lines 5-9, 25) which means the phase detector is a sampling phase detector. However, Vorenkamp does not specifically disclose a sampling phase detector.

Dacus, in the same kind of invention, discloses a PLL frequency synthesizer (abstract, fig. 19) wherein the PLL including a sampling phase detector (column 21 line 45 to column 22 line12). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have Vorenkamp, modified by Dacus to check errors may happen in each pulse in order to prevent the loop from responding to the modulation induced phase error.

Regarding claim 9, this claim is rejected for the same reason as set forth in claim 1, wherein the signal converts from the reference signal is a harmonic signal and the phase error signal is generated from the harmonic signal (column 5 line 47 to column 6 line 67), wherein the harmonic signal has a rising/falling edge (fig.2, column 49 line 23) wherein converting the reference signal is performed by cascaded amplification stage (column 23 lines 38-53, column 24 lines 19-54, figs. 12-16).

Regarding claim 17, this claim is rejected for the same reason as set forth in claim 1, wherein a local oscillator comprising a reference oscillator for generating a reference signal and oscillator for generating an oscillator signal (figs.17-18).

Regarding claim 20, this claim is rejected for the same reason as set forth in claims 4 and 17,

Regarding claim 26, this claim is rejected for the same reason as set forth in claim 9, wherein Vorenkamp further discloses a mixer coupled to the local oscillator and the phase detector in a receiver (figs.5, 17-18).

Regarding claim 29, this claim is rejected for the same reason as set forth in claims 4 and 26.

Regarding claims 2-3, 18-19, and 27-28, Vorenkamp further discloses the amplifier comprises a saturated amplification stage (column 23 lines 12-22) and wherein the amplifier comprises a first saturated amplification stage (e.g., 1352 of fig.13) and a second saturated power amplification stage (e.g., 1354 of fig.13).

Regarding claims 6-7, 22, and 31, Vorenkamp further discloses said amplifier comprises balanced outputs (column 23 line 63).

Regarding claims 8, 16, 23, and 32, Vorenkamp discloses a potentiometer for setting changes the signal level (fig. 35, column 40 lines 5-18).

Regarding claim 10, Vorenkamp further disclose the harmonic-rich signal is a substantially square-wave signal (column 23 line 20).

Regarding claims 13-15, Vorenkamp further disclose the harmonic-rich signal to first and second harmonic-rich signals (the I and Q signals) cycling with substantially opposite phases (column 34 lines 30-49, column 52 lines 21-34), and Vorenkamp further discloses a weighted portions are added to generate the phase error signal (column 32 lines 5-7).

Regarding claims 24-25 and 33-34, Vorenkamp further discloses a crystal oscillator (fig.17, column 22 line 65) and a dielectric resonator oscillator (column 17 lines 9-22, 50-65).

3. Claims 5, 21, and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Vorenkamp et al. (6,591,091) in view of Dacus et al. (6,172,579) as applied to claims 4, 20, and 29, respectively, above, and further in view of Grondahl (5,953,645).

Regarding claim 5, 21, and 30, the modified Vorenkamp discloses the phase locked loop synthesizer having the sampling phase detector for generating a balanced output. It should be noted that in order to have the balance output in a phase detecting circuit, it is obvious the phase detecting circuit including an impedance matching between the input/output. However, the modified Vorenkamp does not specifically disclose the step of matching impedances between input/output.

Grondahl discloses a sampling phase detector (title) including the step of matching impedance between an input and an output (column 2 lines 15-60). Therefore, it would have been obvious to have the modified Vorenkamp, modified by Grondahl to prevent a mismatch between an input and an output in order to improve an electronic device having a multiple-band signal.

Response to Arguments

4. Applicant's arguments with respect to claims 1-10, 13-34 have been considered but are moot in view of the new ground(s) of rejection.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Simon Nguyen whose telephone number is (703) 308-1116. The examiner can normally be reached on Monday-Friday from 7:00 AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban, can be reached on (703) 305-4385.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 306-0377.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314, (for formal communications intended for entry)

Hand-delivered response should be brought to Crystal Park II,

2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Simon Nguyen

February 9, 2004